What is claimed is:

1.   1. A method for automatically generating a test environment for testing a plurality of DUTs in a

2.   test system, comprising the steps of:

3.   mapping the plurality of DUTs into pins of the tester system to create pin data;

4.   inputting into a test program generator pattern data, generic test program rules and the pin data;

5.   generating a multi-DUT test program and multi-DUT pattern data; and

6.   controlling the test system through the test program.

1.   2. The method of claim 1 also comprising the step of generating functional fail data for each

2.   DUT.

1.   3. The method of claim 1 wherein the multi-DUT test program makes a plurality of DUTs appear

2.   as a single DUT.

1.   4. The method of claim 1 wherein test program generation occurs independently from tester

2.   software.

1.   5. The method of claim 1 wherein the mapping of the plurality of DUTs to the tester system pins

2.   occurs independently of restrictions imposed by the test system.

1.   6. The method of claim 5 also comprising the step of interfacing to a generic device interface

2.   board based on channel assignments created in the mapping step.

1.   7. An automated test system which generates test results for a plurality of DUTs using one

2.   tester, which automated test system comprises.

3.   a pin data storage area which contains pin data which maps the plurality of DUTs into pins of the

4   tester system;

5   a pattern data storage area,

6   a generic program rules storage area;

7   a test program generator which takes as input the pin data, pattern data and generic program

8   rules;

9   a multi-DUT test program which is generated by the test program;

10   a multi-DUT pattern data storage area generated by the the test program;

11   a tester containing a plurality of DUTs that has an input from the multi-DUT pattern data and is

12   controlled by the multi-DUT test program.

1   8. The automated test system of claim 7 which also comprises a storage area for receiving fail

2   data for each of the plurality of DUTs.

1   9. The automated test system of claim 7 where the multi-DUT pattern data is input into the tester

2   in either serial or parallel form.

1   10. The automated test system of claim 7 where the multi-DUT pattern data appears to the tester

2   as a pattern data from a single DUT.

1   11. The automated test system of claim 7 where pin data in the pin data storage area is mapped in

2   a manner that would violate tester pin restrictions.

1   12. The automated test system of claim 7 also comprise a generic device interface board that is

2   mapped to the tester according to the pin data.

1   13. A program storage device readable by automated test system, tangibly embodying a program

2   of instructions executable by the automated test system to perform method steps for automatically

3   generating a test environment for testing a plurality of DUTs in a tester, said method steps

4   comprising:

5   mapping the plurality of DUTs into pins of the tester system to create pin data;

6   inputting into a test program generator pattern data, generic test program rules and the pin data;

7   generating a multi-DUT test program and multi-DUT pattern data; and

8   controlling the tester through the test program.

1   14. The program storage device of claim 13 wherein the method also comprises the step of

2   generating functional fail data for each DUT.

1   15. The program storage device of claim 13 wherein the multi-DUT test program makes a

2   plurality of DUTs appear as a single DUT.

1   16. The program storage device of claim 13 wherein test program generation occurs

2   independently from tester software.

1   17. The program storage device of claim 13 wherein the mapping of the plurality of DUTs to

2   tester system pins occurs independently of restrictions imposed by the test system.

1   18. The program storage device of claim 13 wherein the multi-DUT test patterns are provided to

2   the tester in both serial and parallel form.